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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/749,590	OHTAKE ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-17,22-26 and 28-30* is/are pending in the application.

4a) Of the above claim(s) *2,4,8,10-17 and 23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,7,9,22,24-26 and 28-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Amendment filed May 19, 2004 has been entered. Claims 1-4, 24 and 26 have been amended. Claim 27 has been canceled. Claims 1-4, 7-17, 22-26 and 28-30 are pending. The following claims have been withdrawn from consideration: non-elected invention, claims 11-17, species, claims 2, 4, 8 and 23. The action on merits of claims 1, 3, 7, 9, 22, 24-26 and 28-30 follows.

Claim Objections

2. Claims 3 and 26 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

The limitation of claims 3 and 26: "the silicon oxide film is a native oxide film or a chemical oxide film" has already been claimed by claims 1 and 24. Since the claims are directed a semiconductor device, thus no matter how the oxide film is made, the structure is still an oxide.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 3, 7, 9, 22, 24-26 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over K. Kasai et al. *W/WN$_x$/Poly-Si Gate Technology for Future High Speed Deep*

Submicron CMOS LSIs, in view of Jeng et al. (U.S. Patent No. 5,877,074) and Tsukamoto (U.S. Pub No. 2001/0000629) all of record.

With respect to claim 1, Kasai teaches a semiconductor device substantially as claimed including:

a pair of impurity diffused regions formed in a silicon substrate, spaced from each other; and

a gate electrode formed above the silicon substrate between the pair of impurity diffused regions with a gate insulation film interposed therebetween, the gate electrode being formed of a first polycrystalline silicon film formed on the gate insulation film and doped with boron, a second polycrystalline silicon film formed on the first polycrystalline silicon film having a thickness and having crystal grain boundaries which are discontinuous to the first polycrystalline silicon film, and a metal nitride film (WN_x) formed on the second polycrystalline silicon film,

the second polycrystalline silicon film being for preventing boron in the first polycrystalline silicon film from diffusing toward the metal nitride film. (See Figs. 2-3).

Thus, Kasai is shown to teach all the features of the claim with the exception of the second polycrystalline silicon film having a thickness thinner than that of the first polycrystalline silicon film and an oxide film formed on the first polycrystalline silicon film.

With respect to the thickness of the polycrystalline silicon films, Jeng teaches a semiconductor device including: a gate electrode formed above the silicon substrate (11) with a gate insulation film (12) interposed therebetween, the gate electrode being formed of a first polycrystalline silicon film (31) formed on the gate insulation film (12), a second polycrystalline

silicon film (32) formed on the first polycrystalline silicon film (31), having a thickness of that is thinner than that of the first polysilicon layer (31). (See Fig. 5, col. 3, ll. 5-19).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the second polycrystalline silicon film of Kasai to the thickness thinner than that of the first polysilicon layer as taught by Jeng to prevent impurity atoms from out diffusion during the formation of the metal layer (W).

With respect to the oxide film, Tsukamoto teaches a MOSFET having two layers of polycrystalline silicon films (6 and 7) including: an oxide film (20) formed on the first polycrystalline silicon film (6). (See Fig. 6, also Summary of the Invention).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form an oxide film between the first and second polycrystalline silicon films of Kasai as taught by Tsukamoto to suppress fluctuation in the threshold voltage V_{th}.

Regarding the functional limitation of "the second polycrystalline silicon film being for preventing boron in the first polycrystalline silicon film from diffusing toward the metal nitride film", since the crystalline of the polysilicon has been disrupted by the formation of the second polycrystalline silicon layer, thus, the second polycrystalline of Kasai meet the functional limitation as claimed.

With respect to claim 24, Kasai teaches a semiconductor device substantially as claimed including:

a pair of impurity diffused regions formed in a silicon substrate, spaced from each other; and

a gate electrode formed above the silicon substrate between the pair of impurity diffused regions with a gate insulation film interposed therebetween, the gate electrode being formed of a first polycrystalline silicon film formed on the gate insulation film and doped with boron, a second polycrystalline silicon film formed on the first polycrystalline silicon film having a thickness and having crystal grain boundaries which are discontinuous to the first polycrystalline silicon film, and a metal nitride film (WN_x) formed on the second polycrystalline silicon film. (See Figs. 2-3).

Thus, Kasai is shown to teach all the features of the claim with the exception of the second polycrystalline silicon film having a thickness of 2-20 nm and thinner than that of the first polycrystalline silicon film and a silicon oxide film formed on the first polycrystalline film. The claimed thickness of the second polycrystalline silicon film does not appear to be critical.

Note that the specification contains no disclosure of either the critical nature of the claimed *thickness (2-20 nm)* of any unexpected results arising therefrom. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

However, with respect to the thickness of the polycrystalline silicon films, Jeng teaches a semiconductor device including: a gate electrode formed above the silicon substrate (11) with a gate insulation film (12) interposed therebetween, the gate electrode being formed of a first

polycrystalline silicon film (31) formed on the gate insulation film (12), a second polycrystalline silicon film (32) formed on the first polycrystalline silicon film (31) having a thickness of 20-40 nm and thinner than that of the first polysilicon layer (31) (110-130nm). (See Fig. 5, col. 3, ll. 5-19).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the second polycrystalline silicon film of Kasai to the thickness thinner than that of the first polysilicon layer as taught by Jeng to prevent impurity atoms from out diffusion during the formation of the metal layer (W).

The thickness of the second polysilicon layer (32) of Jeng meet the upper limit of the claimed range.

Regarding the second polycrystalline silicon film (32), the subsequent annealing process has crystallized the deposited α-Si. Further, although Jeng discloses that polysilicon 31 is doped with phosphorous, it is well known in the art that the discloses device of Jeng is an n-gate (see Kasai, Fig. 3). Therefore, to form a p-gate, the dopant will be boron or p-type dopants.

With respect to the oxide film, Tsukamoto teaches a MOSFET having two layers of polycrystalline silicon films (6 and 7) including: an oxide film (20) formed on the first polycrystalline silicon film (6). (See Fig. 6, also Summary of the Invention).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form an oxide film between the first and second polycrystalline silicon films of Kasai as taught by Tsukamoto to suppress fluctuation in the threshold voltage V_{th}.

With respect to claims 3 and 26, as best understood by the examiner, the oxide of Tsukamoto is silicon oxide film.

Product by process limitation:

The expression "the silicon oxide is a native oxide film or a chemical oxide film" is taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

With respect to claims 7, 28 and 30, the first (6) and second (7) polycrystalline silicon film of Tsukamoto are further doped with boron. Further, the native oxide layer (20) formed between the two polycrystalline silicon films (6, 7) functions as impurities diffusion blocker (suppress fluctuations in the threshold voltage V_{th} caused by mutual diffusion of the impurities) and following an anneal step, the boron impurities are known to out diffuse, segregate toward the upper surface, therefore, the boron (impurity) concentration in the first polycrystalline silicon film (6) near the interface between the first polycrystalline silicon film (6) and the second polycrystalline silicon film (7) is inherently higher than boron (impurity) concentration in the

second polycrystalline silicon film (7) near an interface between the first polycrystalline silicon film (6) and the second polycrystalline silicon film (7) or another word, boron at the top of the first polysilicon layer is higher than that at the bottom of the second polysilicon layer.

With respect to claims 9 and 29, in view of Tsukamoto, the crystal grain size of the first polycrystalline silicon film (6) is smaller than that of the second polycrystalline silicon film (7).

With respect to claims 22 and 25, the semiconductor device of Kasai further includes a metal film (W) formed on the metal nitride film (WN).

Response to Arguments

4. Applicant's arguments filed May 19, 2004 have been fully considered but they are not persuasive.

With respect to the combination of the references, the Applicants conclude: thus, there would be no motivation to combine the references as asserted by the examiner.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation to combine are provided by the references for instant, Tsukamoto teaches that the present of the oxide at the interface of two polysilicon layers would suppress the

diffusion of boron therefore, the fluctuation of the threshold voltage can be suppressed. (see[0028]).

5. In response to applicant's argument that Jeng relates not to the dual gate structure but to the single gate structure, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

With respect to the diffusion of boron, Applicants appear to contend that the thinness (2-20nm) of the second polysilicon is the main reason that prevent the diffusion of boron. However, it is known from Kasai, Jeng, Tsukamoto and also the present disclosure that the crystal discontinuity between the polysilicon layers is one of the main reason. Secondly, in view of Tsukamoto, the present of the oxide film at the interface between the discontinuous crystal polysilicon layers can suppress the diffusion more effectively. Thus, the thinness of the second polysilicon only contribute to the high of the MOSFET.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 9:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anh D. Mai
July 13, 2004